187. (Amended) The method of claim 184 further including:

receiving a second read request from the bus controller wherein the block size information and the second read request are included in the same request;

outputting the first amount of data corresponding to the block size information onto the bus in response to the second read request; and

wherein the memory device outputs the data synchronously with respect to the external clock signal, during a plurality of clock cycles of the external clock signal and in accordance with the value stored in the time delay register.

REMARKS

This Amendment seeks to place this application in condition for allowance. Several of the pending claims have been amended in order to more fully and/or definitely claim Applicants' invention. The specification has been amended to identify the continuation or related U.S. application data upon which priority is claimed. A new Abstract of the Disclosure is presented to more fully reflect the invention claimed herein. Finally, the drawings have been amended (i.e., added new Figure 16) to more fully illustrate the features of the claimed invention (See, 37 C.F.R. §1.83(a)) and the specification has been amended to correspond to new Figure 16. No new matter has been added.

Office Action

In the Office Action mailed July 16, 1999, claims 151-157, 161-163, 165, 168-173, 177-179 and 181 were rejected as being anticipated by Jackson (U.S. Patent 4,315,308; hereinafter "Jackson" or "the Jackson patent"). Several of the claims were objected to as being dependent upon the rejected claims. Finally, claims 184-188 were found to be allowable.

The Jackson Patent

Jackson discloses a system including a microprocessor 200, a bus interface unit 201, and peripheral units (e.g., memory). Microprocessor 200 is connected to bus interface unit 201, via interface lines, i.e., clock line CLK A, ACD bus 214, ISA 215, and ISB 216. (Jackson, Fig. 1 and col. 4, lines 33-44). Bus interface unit 201 is connected to the peripheral units. (Jackson, Fig. 1 and 6). Microprocessor 200 communicates with the peripheral units by means of bus interface unit 201. (Jackson, Fig.1, and col. 4, lines 33-37). In this regard, the bus interface unit 201 provides interface control of data transfers between the microprocessor 200 and the peripheral units (Jackson, col. 4, lines 16-21), and, in particular, includes circuitry/means to:

(1) receive and decode instructions (e.g., a read data from memory instruction as well as data length transfer information) from the microprocessor 200; (See, e.g., Jackson, col. 8, lines 46-60 and Figs. 6 and 7);

(2) control the memory by asserting the proper control signals in conjunction with generating and applying address signals

necessary to provide the requested number of bytes of data corresponding to the data length transfer information (i.e., bits 10, 11 and 12 in the control specification), (See, e.g., Jackson, col. 8, line 58 to col. 9, line 15, and Figs. 3 and 6);

(3) fetch and buffer data returned from the memory or memory module in response to the read data instruction, (Jackson, col. 6, lines 8-12; col. 8, lines 65-68; and col. 9, line 37-40); and

(4) transfer that data to the microprocessor 200 using control signal ISB to synchronize that transfer relative to clock signal CLK A. (See, e.g., Jackson, col. 6, lines 8-12; col. 9, line 37-44; and Fig. 7).[1]

Although Jackson does not describe the memory or memory modules in any detail, it is most likely that the memory devices, and modules containing those devices, were standard, off-the-shelf components. That is, standard, off-the-shelf memory devices and standard-off-the-shelf memory modules incorporating such devices, for example, memory devices like those described in the Kung et al., U.S. Patent 4,449,207, Voss, U.S. Patent 4,646,279 and Hardee et al., U.S. Patent 5,077,693. These memory devices employ such signals as OE\, CS\, RAS\, CAS\ and address signals.

Thus, neither the microprocessor 200 nor the bus interface unit 201 in Jackson provide data length transfer information to the memory devices or to the memory devices on the memory modules.

---

[1] It should be noted that claims 3, 4, 7 and 8 of the Jackson patent also describe the means of, and functions performed by, the bus interface unit. (Col. 11, lines 3-27 and Col. 12, lines 29-55.

Rather, the bus interface unit 201 receives and decodes that information, and, based thereon, generates and applies the addresses and control signals (i.e., OE\, RAS\, CAS\) necessary to obtain the number of bytes of data defined by data length transfer information. (See, e.g., Jackson, col 8, lines 57-62; col. 9, lines 1-15 and Figs. 6 and 7).

Moreover, it appears that the memory devices or memory modules employed in Jackson do not receive the clock signal (CLK A) nor do they provide data synchronously with respect to that clock signal. Instead, the bus interface unit 201 fetches the data returned from the memory, buffers and aligns that data, and then transfers it to the microprocessor 200, using control signal ISB to synchronize data transfer relative to CLK A. (See, e.g., Jackson, col. 6, lines 8-12; col. 8, lines 65-68; col. 9, line 37-44 and Fig. 7).

Jackson Does Not Anticipate Claim 151

Amended claim 151 is a method of controlling a synchronous memory device. Amended claim 151 requires, among other things, the memory device to be provided first block size information. The first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request. In addition, claim 151 further requires the memory device to output the first amount of data corresponding to the first block size information, in response to a read request, onto the bus synchronously with respect to an external clock signal.

As mentioned above, the data length transfer information in Jackson is not provided to the memory devices. Instead, the bus

interface unit 201 receives and decodes that information, and, based thereon, generates the addresses and control signals necessary to obtain the amount of data defined by data length transfer information.

Further, the memory devices employed in Jackson did not provide data synchronously with respect to the external clock signal. Rather, bus interface unit 201 buffers the data and gates that data to the microprocessor 200 -- using control signal ISB to synchronize data transfer relative to clock signal CLK A.

Thus, for at least those reasons, Jackson does not anticipate amended claim 151 or the claims which depend therefrom (i.e., claims 152-157, 161-163, and 165).

Jackson Does Not Anticipate Claim 168

Amended claim 168 is a method of operation of a synchronous memory device. The method requires, among other things, the memory device to receive first block size information from a bus controller. Like in claim 151, the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request.

The method also requires, the memory device to output the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal. In claim 168, the memory device receives the external clock signal.

For reasons similar to those mentioned above with respect to claim 151, the memory devices in Jackson do not receive data length

transfer information. Further, the memory devices in Jackson do not receive the clock signal (CLK A) nor do they provide data synchronously with respect to the clock signal CLK A.

Thus, for at least those reasons, Jackson does not anticipate amended claim 168 or the claims which depend therefrom (i.e., 169-173, 177-179, and 181).

Amendment to the Specification

The specification has been amended to identify the continuation or related U.S. application data of this application. No new matter has been added. In short, this application is a continuation of Application No. 09/196,199, filed on November 20, 1998 (still pending), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned). As such, the instant application is entitled to an April 18, 1990 priority date.

Moreover, the specification has been amended to correspond to new Figure 16 -- as is discussed immediately below. No new matter has been added.

Amendment to the Drawings

New Figure 16, attached hereto, is added to illustrate, among other things, access-time register(s) 173. Figure 16 illustrates one embodiment of the internal registers within each device illustrated in Figure 2. Support may be found in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

The specification has been amended to correspond to new Figure 16. No new matter has been added.

By way of note, the amendment to the drawings and the corresponding amendment of the specification is similar to the amendment made in the application leading to U.S. Patent 5,841,580. The '580 patent is the parent of the instant application.

Abstract of the Disclosure

A new Abstract of the Disclosure is attached hereto. No new matter has been added.

Draftperson's Objections

The Draftperson's objections to the drawings are noted. Applicants request that these objections be held in abeyance until this application is found to be in condition for allowance.

Information Disclosure Statements

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicants submitted on June 11, 1999, a modified Form PTO-1449, including a copy of the documents cited therein.

(See copy of stamped Postcard receipt, attached hereto). It appears from the Office Action Summary, that the Examiner has not yet received Applicants' June 11 Information Disclosure Statement. A copy of that Information Disclosure Statement is attached hereto.

In addition, Applicants submit herewith a third Information Disclosure Statement. The fee as prescribed in 37 C.F.R. §1.17(p) accompanies this Statement. (See, 37 C.F.R. §1.97(c)).

As stated in the Information Disclosure Statements, it is believed that the Examiner may find the documents cited in the Form PTO-1449 material to the patentability of one or more of the claims in the above-referenced application. As such, it is respectfully requested that the Examiner make his consideration of the documents cited in the Form PTO-1449 formally of record with the next Action.

CONCLUSION

Applicants respectfully request entry of the foregoing amendment. Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of Applicants' invention. Applicants respectfully request reconsideration and allowance of all claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 703-787-9636.

Respectfully submitted,

Date: July 23, 1999

Neil A. Steinberg
Reg. No. 34,735
703-787-9636